PATENT ABSTRACTS OF JAPAN

(11) Publication number : 05-003183
(43) Date of publication of application : 08.01.1993

(51) Int.Cl. H01L 21/304
H01L 21/321

(21) Application number : 03-153650
(22) Date of filing : 26.06.1991

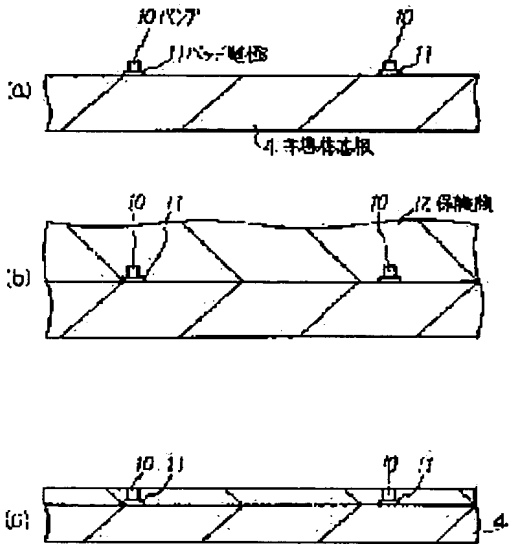
(71) Applicant : NEC CORP
(72) Inventor : URUSHIMA MICHITAKA

(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57) Abstract:

PURPOSE: To enable a semiconductor substrate to be enhanced in mechanical strength and lessened in thickness by a method wherein a protective film is provided to the semiconductor substrate to cover its surface including the side faces of bumps provided to pad electrodes, and the upside of the protective film is set level with those of the bumps so as to enable the upsides of the bumps to be exposed.

CONSTITUTION: Pad electrodes 11 electrically connected to the outside are provided onto a semiconductor substrate 4 where semiconductor elements are formed, a metal film of Ti or the like is formed on the surface of the substrate 4 including the pad electrodes 11, the pad electrodes 11 are selectively plated with Au or the like making the metal film serve as a plating electrode, then the metal film is removed, and bumps 10 are formed. Then, a protective film 12 of epoxy resin or the like is applied onto all the surface of the substrate 4 including the bumps 10 as thick as 200μm and then cured. In succession, the semiconductor substrate 4 is rendered as thin as 200μm or so by grinding its rear side, and furthermore the protective film 12 is etched back to be as thin as 20μm or so to make the upsides of the bumps 10 exposed.



LEGAL STATUS

[Date of request for examination] 30.06.1995

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 2701589

[Date of registration] 03.10.1997

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by having the protective coat to which the front face containing the side face of the pad electrode prepared on the semiconductor substrate, the bump who prepared on the aforementioned pad electrode, and the aforementioned bump was covered, and the aforementioned bump's top was exposed for the top as the same flat surface as the aforementioned bump's top.
[Claim 2] The semiconductor device according to claim 1 with the thickness of a semiconductor substrate thinner than the thickness of a protective coat.
[Claim 3] The process which prepares the pad electrode for external connection on the semiconductor substrate which prepared the semiconductor device, deposits a metal layer alternatively on the aforementioned pad electrode, and forms a bump, The manufacture technique of the semiconductor device characterized by including the process which forms a protective coat in the front face including the aforementioned bump, the process which carries out the grinding of the rear face of the aforementioned semiconductor substrate, and makes thickness of the aforementioned semiconductor substrate thin, and the process at which the grinding of the aforementioned protective coat is carried out, and the aforementioned bump's top is exposed.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] this invention relates to a semiconductor device and its manufacture technique.
[0002]
[Description of the Prior Art] the semiconductor substrate 4 top in which the semiconductor device was formed as the manufacture technique of the conventional semiconductor device was first shown in drawing 3 (a) -- the electrical installation with the exterior -- ****** -- the pad electrode 11 of a sake is formed alternatively
[0003] Next, as shown in drawing 3 (b), after depositing the metal membranes 14, such as Ti, Cr, and Cu, on the front face of the semiconductor substrate 4 containing the pad electrode 11, the bumps 10, such as Au, Cu, and Pb-Sn, are alternatively formed on the metal membrane 14 on the pad electrode 11 using photo-lithography technique and the galvanizing method.
[0004] Next, as shown in drawing 3 (c), the etching elimination of the metal membrane 14 was carried out, having used the bump 10 as the mask, and the semiconductor device was constituted.
[0005] A flip chip is in one of technique which mounts the semiconductor device which has such a bump. This is connected by carrying out solder fusion of the bump 10 who consists of a bonding pad 13, Pb-Sn, etc. of the package substrate 15, as shown in drawing 4 (a). Subsequently, it covers with the resin layers 17, such as an epoxy resin, for protection of a semiconductor device.
[0006] Moreover, there is a tape carrier package method as technique of mounting the semiconductor substrate 4 which has a bump similarly. This connects a bump 10 and the inner lead 6 on a tape carrier package tape using thermocompression bonding or a eutectic method, as shown in drawing 4 (b) (Inner Lead Bonding). Next, the resin layers 17, such as an epoxy resin, are dropped at semiconductor substrate 4 front face for the purpose of enhancement and mechanical protection of a reliability, for example, the resin seal of the semiconductor chip front face is carried out. Subsequently, an electric check and a burn-in test are performed using the pad for electric sorting 9. Furthermore, when it mounts in a package substrate, after cutting and fabricating an outer lead 7 in a predetermined dimension, bonding of the bonding pad 13 and the outer lead 7 of the package substrate 15 is carried out, and they are mounted.
[0007]
[Problem(s) to be Solved by the Invention] the semiconductor device mentioned above -- the package second half of a flip chip method -- a conductor -- it is very difficult to fill up completely the resin layer formed as protection of an element between a package substrate and a semiconductor substrate, and it is difficult to check this further Moreover, 500 micrometers and a resin layer thickness are 100-300 micrometers, and, as for the conventional semiconductor device, the thickness of a semiconductor substrate has the thickness of 600-800 micrometers collectively. In connection with lightweight-izing and thin-shape-izing of an electronic instrument, the further thin shape-ization of a coming [it] semiconductor device is demanded. That is, it is necessary to make thickness of about 800 micrometers still thin. Therefore, although there is the technique of carrying out the grinding of the semiconductor substrate, it results in a crash of a crack etc. in many cases. Moreover, also about resin thickness, in order to cover a semiconductor device front face completely, the resin of a certain constant rate needed to be dropped and the limitation was in thin shape-ization.

[0008]
[Means for Solving the Problem] The semiconductor device of this invention has the protective coat to which the front face containing the side face of the pad electrode prepared on the semiconductor substrate, the bump who prepared on the aforementioned pad electrode, and the aforementioned bump was covered, and the aforementioned bump's top was exposed for the top as the same flat surface as the aforementioned bump's top.
[0009] The process which the manufacture technique of the semiconductor device of this invention prepares the pad electrode for external connection on the semiconductor substrate which prepared the semiconductor device, deposits a metal layer alternatively on the aforementioned pad electrode, and forms a bump, It is constituted including the process which forms a protective coat in the front face including the aforementioned bump, the process which carries out the grinding of the rear face of the aforementioned semiconductor substrate, and makes thickness of the aforementioned semiconductor substrate thin, and the process at which the grinding of the aforementioned protective coat is carried out, and the aforementioned bump's top is exposed.
[0010]
[Example] Next, this invention is explained with reference to a drawing.
[0011] Drawing 1 (a) - (c) is the cross section of a semiconductor chip shown in the order of the process for explaining the manufacture technique of one example of this invention.
[0012] As shown in drawing 1 (a), on the front face which forms the pad electrode 11 for performing electrical installation with the exterior on the semiconductor substrate 4 which formed the semiconductor device according to the same process as the conventional example, and contains the pad electrode 11 first, for example Metal membranes (not shown), such as Ti, Cr, and Cu, are formed, subsequently to the pad electrode 11 top, a metal membrane is removed and a bump 10 is formed, after galvanizing a metal membrane for Au, Cu, Pb-Sn, etc. alternatively as a plating electrode. In addition, this bump formation as indicated by JP,49-52973,A other than the galvanizing method The wire-bonding method is used for the wire which consists of Au, Pb-Sn, etc. Ball formation can be carried out, it can leave only the ball after a junction for a ball on a pad, and the conventional bump forming methods, such as the technique of forming a bump and technique which is immersed into fusion solder and forms a solder bump only on a pad electrode, can be used by cutting a wire.
[0013] Next, the protective coats 12, such as a ******** resin, are applied in thickness of 200 micrometers, and drawing 1 (b) is made to harden them all over the ** substrate [semiconductor] 4 top including a bump 10 like.
[0014] Next, as shown in drawing 1 (c), the grinding of the rear face of the semiconductor substrate 4 is carried out, thickness of a semiconductor substrate is made thin to about 200 micrometers, further, etchback of the protective coat 12 is carried out until resin thickness is set to about 20 micrometers, and a bump's 10 top is exposed. In addition, in consideration of the thermolysis nature of the semiconductor substrate 4, a bump's 10 height is beforehand made high by forming a ball bump in three-fold [a duplex and] etc., resin thickness may be made thick about 100 micrometers for an intensity at a ** sake, and the semiconductor substrate 4 may be made thin about 50 micrometers.
[0015] Drawing 2 (a) and (b) are the cross sections showing the package status of the semiconductor device of this invention.
[0016] Drawing 2 (a) is an example of a package by the flip chip method, and mounts a semiconductor device through the 2nd bump 16 who prepared on the bump 10 who exposed, or the bonding pad 13 of the package substrate 15.
[0017] Although a bump's 16 method of forming has the galvanizing method and the ball bump method like the case where a bump is formed on a semiconductor substrate here In addition, as indicated by the "Nikkei micro device" July, 1989 issue and 43-65 pages There are technique of applying conductive pastes, such as Ag paste, further on Au bump, the technique of forming conductive resin with printing or a dropping test, etc., and it can carry out easily using the conventional bump forming method. Moreover, pin minute instead of and lead minute instead of of a bump can also be used. Next, in the case of solder-solder, the technique of connection, for example, the combination of the denudation bump 10 and the 2nd bump 16, connects by fusion, in Au-Au, it

connects using a different direction conductivity sheet, and, in the case of an electroconductive glue, a suitable connection method is chosen by the bump material, such as connecting by hardening.
[0018] Drawing 2 (b) is an example of a package using the tape carrier package tape, forms the 2nd bump 16 in the bump 10 top who exposed to the protective coat 12, or the inner lead section, and carries out inner lead bonding by thermocompression bonding etc. Subsequently, outer lead bonding is carried out by thermocompression bonding with the outer-lead section 7 by the bonding pad 13 on the package substrate 15. In addition, a bump's 16 formation technique is performed like the case of a flip chip. Furthermore, it is also possible to carry out bonding to the bump 10 who exposed the direct lead, without forming a bump 16. Moreover, it can use also as a semiconductor substrate for the conventional wire-bonding semiconductor devices by carrying out direct wire bonding on the bump 10 who exposed.
[0019]
[Effect of the Invention] As explained above, since this invention becomes possible [making semiconductor machine board thickness still thin compared with the former], the manufacture of a thin shape and a lightweight type semiconductor device of it is attained. Moreover, formation of a protection resin can be performed easily thinly. Although exchange of the individual unit at the time of after [a substrate package] poor occurrence was difficult when covering a resin with the further conventional flip chip method all over a package substrate after a package, a resin seal and since it can mount, in this invention, it also has individually the effect that exchange of an individual unit is possible.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

Effect

[Effect of the Invention] As explained above, since this invention becomes possible [making semiconductor machine board thickness still thin compared with the former], the manufacture of a thin shape and a lightweight type semiconductor device of it is attained. Moreover, formation of a protection resin can be performed easily thinly. Although exchange of the individual unit at the time of after [a substrate package] poor occurrence was difficult when covering a resin with the further conventional flip chip method all over a package substrate after a package, a resin seal and since it can mount, in this invention, it also has individually the effect that exchange of an individual unit is possible.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The cross section of a semiconductor chip shown in the order of the process for explaining the manufacture technique of one example of this invention.
[Drawing 2] The cross section showing the package status of the semiconductor device of this invention.
[Drawing 3] The cross section of a semiconductor chip shown in the order of the process for explaining the manufacture technique of the conventional semiconductor device.
[Drawing 4] The cross section showing the package status of the conventional semiconductor device.

[Description of Notations]
4 Semiconductor Substrate
6 Inner Lead
7 Outer Lead
10, 16 Bump
11 Pad Electrode
12 Protective Coat
13 Bonding Pad
14 Metal Membrane
15 Package Substrate
17 Resin Layer

[Translation done.]

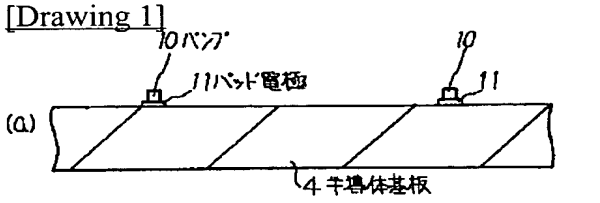
* NOTICES *

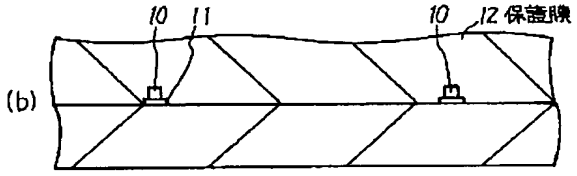
The Japanese Patent Office is not responsible for any damages caused by the use of this translation.

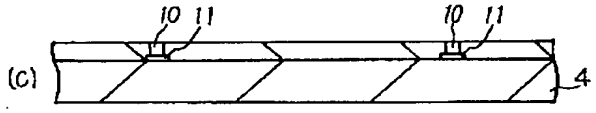
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

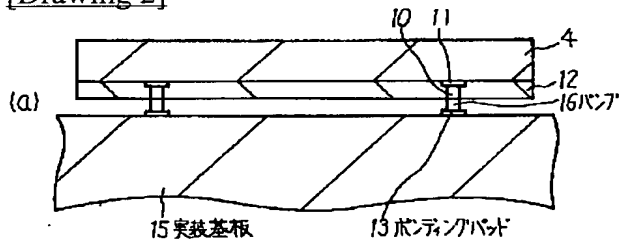
[Drawing 1]

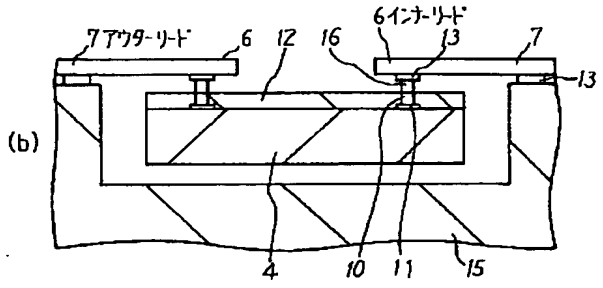




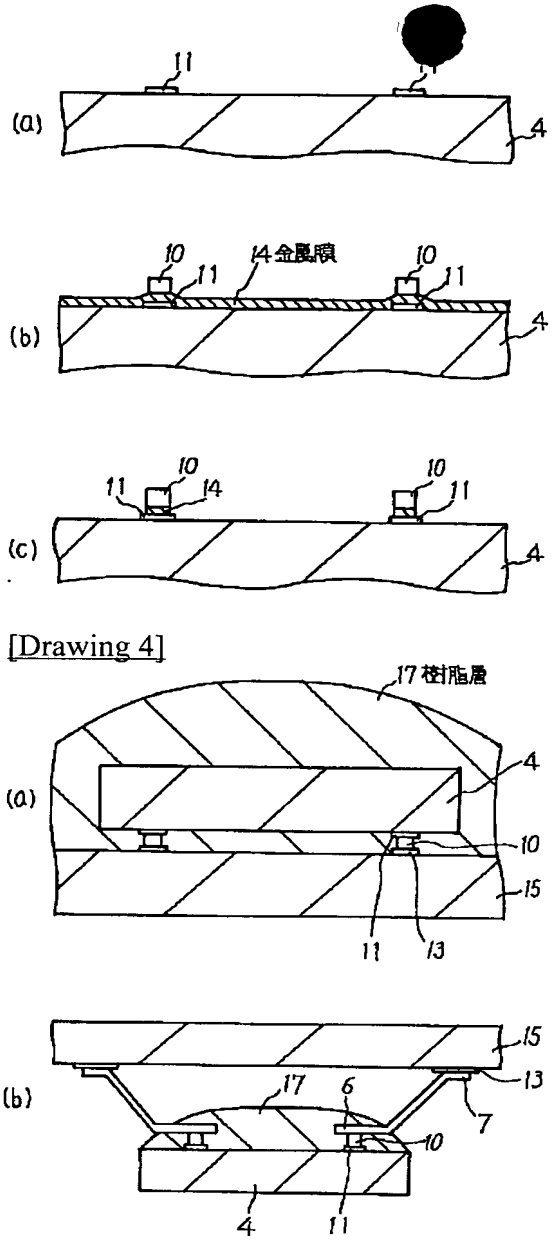


[Drawing 2]





[Drawing 3]



[Drawing 4]

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平5－3183

(43)公開日　平成５年(1993)１月８日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　21/304	３２１　Ｂ	8831－4M		
21/321				
		9168－4M	Ｈ０１Ｌ　21/ 92	Ｆ

審査請求　未請求　請求項の数３(全　４　頁)

(21)出願番号　特願平3－153650

(22)出願日　平成３年(1991)６月26日

(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号

(72)発明者　漆島　路高
東京都港区芝五丁目７番１号日本電気株式会社内

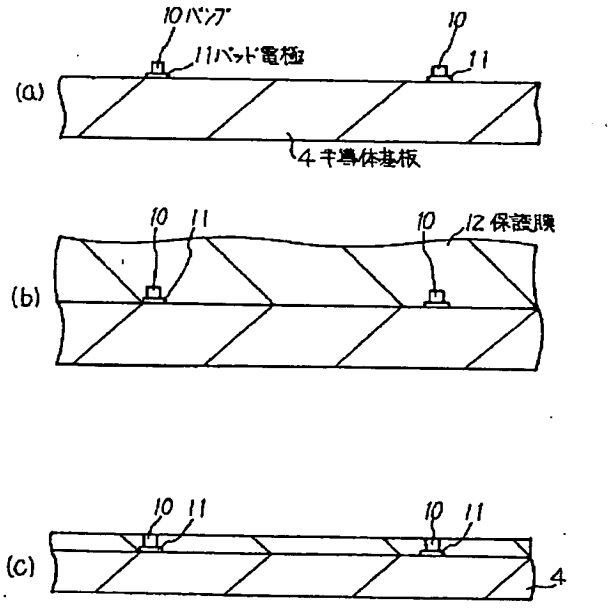
(74)代理人　弁理士　内原　晋

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】

【構成】半導体基板４の上に設けたパッド電極１１の上にバンプ１０を形成し、保護膜１２を塗布して硬化後、半導体基板４の裏面を研削し、次に、保護膜１２をバンプ１０が露出するまで研削する。

【効果】保護膜の形成により、半導体基板の機械的強度を補強して半導体基板の厚さを薄くでき、実装状態の厚さを薄くできる。



1

【特許請求の範囲】

【請求項１】　半導体基板上に設けたパッド電極と、前記パッド電極上に設けたバンプと、前記バンプの側面を含む表面を被覆し且つ上面を前記バンプの上面と同一平面として前記バンプの上面を露出させた保護膜とを有することを特徴とする半導体装置。

【請求項２】　半導体基板の厚さが保護膜の厚さより薄い請求項１記載の半導体装置。

【請求項３】　半導体素子を設けた半導体基板上に外部接続用のパッド電極を設け前記パッド電極上に金属層を選択的に堆積してバンプを形成する工程と、前記バンプを含む表面に保護膜を形成する工程と、前記半導体基板の裏面を研削して前記半導体基板の厚さを薄くする工程と、前記保護膜を研削して前記バンプの上面を露出させる工程とを含むことを特徴とする半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は半導体装置及びその製造方法に関する。

【０００２】

【従来の技術】従来の半導体装置の製造方法は、まず、図３（ａ）に示すように、半導体素子が形成された半導体基板４の上に外部との電気的接続行なうためのパッド電極１１を選択的に形成する。

【０００３】次に、図３（ｂ）に示すように、パッド電極１１を含む半導体基板４の表面にＴｉ，Ｃｒ，Ｃｕ等の金属膜１４を堆積した後、フォトリソグラフィー技術及びめっき法を用いてパッド電極１１上の金属膜１４の上に選択的に、Ａｕ，Ｃｕ，Ｐｂ－Ｓｎ等のバンプ１０を形成する。

【０００４】次に、図３（ｃ）に示すように、バンプ１０をマスクとして金属膜１４をエッチング除去して半導体装置を構成していた。

【０００５】このようなバンプを有する半導体装置を実装する方法の一つにフリップチップがある。これは図４（ａ）に示すように、実装基板１５のボンディングパッド１３とＰｂ－Ｓｎ等からなる、バンプ１０とを半田熔融することにより接続する。次いで、半導体素子の保護のために、エポキシ樹脂等の樹脂層１７で被覆する。

【０００６】また、同様にバンプを有する半導体基板４を実装する方法として、フィルムキャリア方式がある。これは、図４（ｂ）に示すように、バンプ１０と、フィルムキャリアテープ上のインナーリード６を熱圧着法又は共晶法を用いて接続（Ｉｎｎｅｒ　Ｌｅａｄ　Ｂｏｎｄｉｎｇ）する。次に、半導体基板４表面に信頼性の向上及び機械的保護を目的として、例えば、エポキシ樹脂等の樹脂層１７を滴下して、半導体チップ表面を樹脂封止する。次いで、電気選別用パッド９を用いて電気検査及びバーンインテストを行なう。さらに、実装基板に実

2

装する場合は、所定寸法にアウターリード７を切断し、成形した後、実装基板１５のボンディングパッド１３とアウターリード７とをボンディングして実装する。

【０００７】

【発明が解決しようとする課題】上述した半導体装置は、フリップチップ方式の実装後半導体素子の保護として形成する樹脂層が実装基板と半導体基板の間に完全に充填するのが非常にむずかしく、さらにこれを確認することが難しい。又、従来の半導体装置は半導体基板の厚さが５００μｍ，樹脂層の厚さが１００～３００μｍで、全体として６００～８００μｍの厚さを有している。電子装置の軽量化・薄型化に伴なって、これるの半導体装置の更なる薄型化が要求されている。すなわち、８００μｍ程度の厚さをさらに薄くする必要がある。そのために、半導体基板を研削する方法があるが、割れ等の破損に至ることが多い。また樹脂厚についても、半導体素子表面を完全に被覆するためには、ある一定量の樹脂を滴下する必要があり薄型化に限界があった。

【０００８】

【課題を解決するための手段】本発明の半導体装置は、半導体基板上に設けたパッド電極と、前記パッド電極上に設けたバンプと、前記バンプの側面を含む表面を被覆し且つ上面を前記バンプの上面と同一平面として前記バンプの上面を露出させた保護膜とを有する。

【０００９】本発明の半導体装置の製造方法は、半導体素子を設けた半導体基板上に外部接続用のパッド電極を設け前記パッド電極上に金属層を選択的に堆積してバンプを形成する工程と、前記バンプを含む表面に保護膜を形成する工程と、前記半導体基板の裏面を研削して前記半導体基板の厚さを薄くする工程と、前記保護膜を研削して前記バンプの上面を露出させる工程とを含んで構成される。

【００１０】

【実施例】次に、本発明について図面を参照して説明する。

【００１１】図１（ａ）～（ｃ）は、本発明の一実施例の製造方法を説明するための工程順に示した半導体チップの断面図である。

【００１２】まず、図１（ａ）に示すように、従来例と同様の工程により半導体素子を形成した半導体基板４上に、外部との電気的接続を行なうためのパッド電極１１を形成し、パッド電極１１を含む表面に例えば、Ｔｉ，Ｃｒ，Ｃｕ等の金属膜（図示せず）を形成し、次いで、金属膜をめっき電極として選択的にパッド電極１１上に例えばＡｕ，Ｃｕ，Ｐｂ－Ｓｎ等をめつきした後金属膜を除去してバンプ１０を形成する。なお、このバンプ形成は、めっき法の他に、特開昭４９－５２９７３号公報に記載されているように、Ａｕ，Ｐｂ－Ｓｎ等からなるワイヤーをワイヤーボンディング法を使用して、ボール形成し、ボールをパッド上に接合後ボールのみを残し、

ワイヤーを切断することによってバンプを形成する方法や、熔融半田中に浸漬してパッド電極上のみに半田バンプを形成する方法等の従来のバンプ形成法を利用することができる。

【００１３】次に、図１（ｂ）に示ように、バンプ１０を含む半導体基板４上全面に、例えばエポキシ樹脂等の保護膜１２を２００μｍの厚さに塗布し、硬化させる。

【００１４】次に図１（ｃ）に示すように、半導体基板４の裏面を研削して半導体基板の厚さを２００μｍ程度まで薄くし、さらに保護膜１２を樹脂厚が２０μｍ程度になるまでエッチバックしてバンプ１０の上面を露出させる。なお、半導体基板４の放熱性を考慮して、あらかじめ、ボールバンプを２重、３重に形成する等によりバンプ１０の高さを高くしておき、強度を保ために、樹脂厚を１００μｍ程度に厚くし、半導体基板４を５０μｍ程度に薄くしていても良い。

【００１５】図２（ａ），（ｂ）は本発明の半導体装置の実装状態を示す断面図である。

【００１６】図２（ａ）はフリップチップ法による実装例で、露出したバンプ１０上又は、実装基板１５のボンディングパッド１３上に設けた第２のバンプ１６を介して半導体装置を実装する。

【００１７】ここで、バンプ１６の形成法は、半導体基板上にバンプを形成した場合と同様に、めっき法、ボールバンプ法があるが、その他に、「日経マイクロデバイス」１９８９年、７月号、４３～６５頁に記載されているように、Ａｕバンプの上にＡｇペースト等の導電性ペーストを更に塗布する方法や、導電性樹脂を印刷や滴下法により形成する方法等があり、従来のバンプ形成法を利用して、容易に実施できる。また、バンプの代りに微小なピンやリードを用いることもできる。次に、接続の方法、例えば、露出バンプ１０と第２のバンプ１６の組み合わせが、半田－半田の場合は、熔融によって接続し、Ａｕ－Ａｕの場合は、異方導電性シートを用いて接続し、導電性接着剤の場合は、硬化によって接続する等バンプ材料により適切な接続方法を選択する。

【００１８】図２（ｂ）は、フィルムキャリアテープを利用した実装例で、保護膜１２に露出したバンプ１０上又は、インナーリード部に第２のバンプ１６を形成し、インナーリードボンディングを例えば熱圧着法等で実施する。次いで、実装基板１５上のボンディングパッド１３でアウターリード部７と、アウターリードボンディングを例えば、熱圧着法で実施する。なおバンプ１６の形成方法は、フリップチップの場合と同様に行なう。更に、バンプ１６を形成せずに直接リードを露出したバンプ１０にボンディングすることも可能である。また、露出したバンプ１０の上に直接ワイヤーボンディングすることにより、従来のワイヤーボンディング半導体装置用の半導体基板としても、利用することができる。

【００１９】

【発明の効果】以上説明したように本発明は、半導体基板厚を、従来に比べ、さらに薄くすることが可能となるため、薄型及び軽量型の半導体装置の製造が可能となる。又、保護樹脂の形成が容易でかつ、薄くできる。さらに従来のフリップチップ法で実装後、実装基板全面に樹脂を被覆する場合は、基板実装後不良発生時の個別単位の交換が困難であったが、本発明では、個別に、樹脂封止及び実装できることから、個別単位の交換が可能という効果も有する。

【図面の簡単な説明】

【図１】本発明の一実施例の製造方法を説明するための工程順に示した半導体チップの断面図。

【図２】本発明の半導体装置の実装状態を示す断面図。

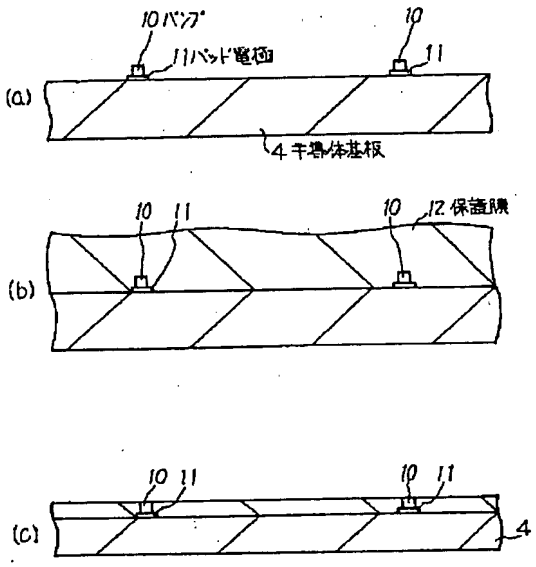
【図３】従来の半導体装置の製造方法を説明するための工程順に示した半導体チップの断面図。

【図４】従来の半導体装置の実装状態を示す断面図。

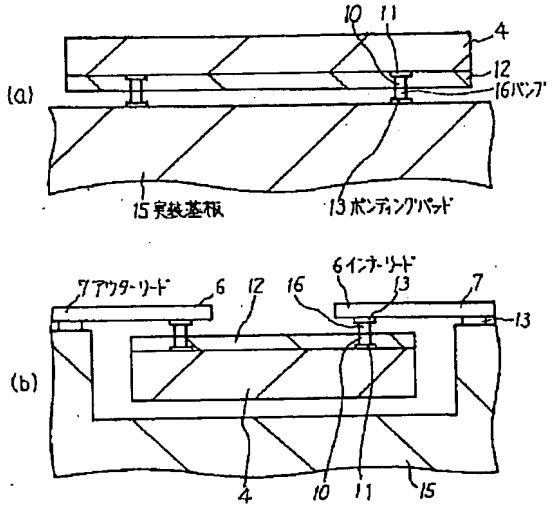
【符号の説明】

４　半導体基板
６　インナーリード
７　アウターリード
１０，１６　バンプ
１１　パッド電極
１２　保護膜
１３　ボンディングパッド
１４　金属膜
１５　実装基板
１７　樹脂層

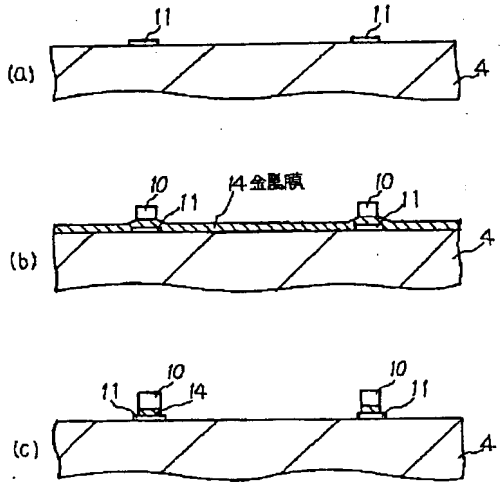
【図１】


10バンプ
11パッド電極
4半導体基板
12保護膜
(a)
(b)
(c)

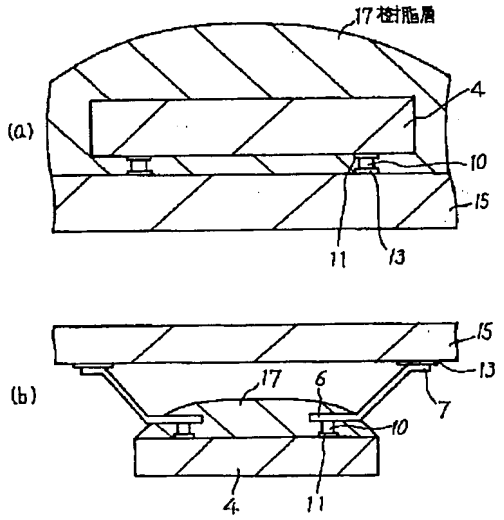
【図２】


16バンプ
15実装基板
13ボンディングパッド
7アウターリード
6インナーリード
(a)
(b)

【図３】


14金属膜
(a)
(b)
(c)

【図４】


17樹脂層
(a)
(b)